R E M A R K S

Applicant has carefully considered the Office Action of August 24, 2004 rejecting all of the claims. The present response is intended to fully address all points of objection raised by the Examiner, and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application are respectfully requested.

A new Power of Attorney is attached to the undersigned, from the inventor and the Assignee. Kindly change the correspondence address accordingly.

A petition for an extension of response time is attached (previously submitted on December 27, 2004).

An additional fee for new claims is attached in a separate paper (previously submitted on December 27, 2004).

The title of the invention has been amended to be more indicative of the invention to which the claims are directed.

The drawings have been amended in a separate paper (attached) to provide clarification of the innovation of the proposed method.

The specification has been amended to provide clarification of the proposed method.

Specifically, page 7, line 1 has been amended to more clearly define the range of the value of n to be a whole number greater than one and the range of the value of k to be a whole number greater than zero. This fact is well-understood to those skilled in the art, since n defines the different number of threads existing in the virtual processor. The parameter k defines the different number of phases within each pipeline. In the case n where equals one, a singlethreaded processor is configured, wherein a

multithreaded processor is configured in the case where n is greater than one. No new matter has been added.

Claims 1 to 10 have been amended. Claim 5 has been deleted. Claims 12 to 23 have been added. Therefore, claims 1 to 23 remain in the case.

The present invention discloses an improved apparatus and method of converting a computer processor configuration into a virtual processor while improving throughput efficiency and resource exploitation by introducing a combination of multithreading and pipeline splitting to an existing and mature computer processor core or to any synchronous logic block. The conversion is achieved in a four-step process: the first step being division of the pipeline phase into a plurality n of sub-phases, the second step being creation of n virtual pipelines comprising n*k sub-phases, the third step being reproduction of register set and the fourth step being adaptation of the register set to enable simultaneous storing of each of the n virtual processor's machine states.

Claim 1 has been amended to more clearly define the components that comprise the computer processor configuration, the components being a register set. This is supported by the specification at page 7, 2ND paragraph, lines 7 to 9, which describe the way the register set is adapted to simultaneously store the thread's multiple machine states.

Claim 1 has also been amended to more clearly define the conversion method, of converting a computer processor configuration into n virtual multithreaded processors, where each of n virtual multithreaded processors is compatible to the computer processor configuration. This is supported by the specification at page 6, 3rd paragraph, line 4, bridging on to page 7, 1st paragraph, line 1.

Claim 1 has also been amended to more clearly define the novelty and non-obvious feature of the inventive process, in achieving a combination of multithreading and pipeline splitting to an existing computer processor configuration, by reproducing the register set and adapting it to simultaneously store the machine states of the n virtual multithreaded processors. This is supported by the specification at page 7, 3rd paragraph, lines 10 and 11, which describe the technique in which the register set is replaced by n identical register sets.

The Examiner has rejected claims 1-3 and 7-11 under Sec. 102(e) as being anticipated by Lauterbach et al.

The process described by Lauterbach relates to a pipeline that is already configured to accept instructions from multiple independent threads of operation. The method divides each pipeline stage into two different stages, where one sub-stage can be processing an instruction from one thread while a second sub-stage is processing an instruction from a different thread. However, Lauterbach discloses nothing regarding a method or apparatus for converting a computer processor configuration into n virtual multithreaded processors while reproducing the register file to support storing and restoring of the multithreads in the processor.

In contrast, the present invention discloses a method and apparatus for converting a computer processor configuration having one or more threads into n virtual multithreaded processors, where each of the n virtual processors is provided to execute the one or more threads and is further compatible to the original computer processor configuration both in instruction set and in execution time.

Furthermore, the present invention describes the manner in which the execution phase is carried out by the

reproduction of the register set and the implementation of selected logic, page 7 and 8, for combining the multithreading procedure and pipeline splitting within an existing and mature computer processor configuration.

The novel technique described herein for improving throughput efficiency and exploiting increased parallelism cannot be considered to be disclosed by Lauterbach. Therefore, independent claims 1 and 12 are not anticipated under Sec. 102.

As stated in the decision in In Re Marshall, 198 USPQ 344 (1978), "To constitute an anticipation, all material elements recited in a claim must be found in one unit of prior art…". Since Lauterbach neither 1) identically describes the invention, nor 2) enables one skilled in the art to practice it, Applicant deems the 102(e) rejection improper, and respectfully requests that it be withdrawn.

The Examiner has rejected claim 4 under Sec. 103(a) as being unpatentable over Lauterbach in view of Hennessy.

Hennessy teaches superpipelining a pipeline processor by increasing the number of pipeline stages and rebalancing the substages, page 510, 3rd paragraph. The technique increases the number of pipeline stages so that it can launch multiple instructions in every pipeline stage.

However, Hennessy discloses nothing regarding the inventive technique of dividing each pipeline phase into a plurality of n sub-phases, wherein the propagation delay of each of the n sub-phases can be less than T/n. For this reason, Hennessy cannot be said to render the invention obvious in combination with Lauterbach, since according to the present invention, it is possible to divide the propagation delay of each of the n sub-phases into non equal sub-phases, where each is less than T/n. This dividing procedure achieves optimization of the complete

converting method by reducing the number of splitting devices without degrading performance.

The Examiner has rejected claims 5 and 6 as being unpatentable over Lauterbach in view of Culler.

Culler describes an interleaved multithreading scheme, whereas the active contexts are supported by replicating the register set and other critical state times, see Culler; The Interleaved Scheme, page 905.

However, Culler suggests nothing about introducing a combination of multithreading and pipeline splitting when converting a computer processor configuration into a virtual multithreaded processor, where the virtual multithreaded processor is compatible to the original computer process configuration in both execution behavior and execution time.

In contrast, the present invention describes the conversion technique by combining multithreading procedure and pipeline splitting, as per the specification, at pages 7 and 8.

Culler adds nothing to the teaching of Lauterbach which would render the present invention obvious, and therefore would not be suitable for to the conversion technique of the present invention.

It is the Applicant's position that the combination of the Hennessy and Lauterbach references as well as the combination of the Culler and Lauterbach references to form the basis of the Sec. 103(a) rejection is improper, and Applicant respectfully requests that it be withdrawn.

Therefore, claims 1 and 12 are deemed to be patentable, and the dependent claims are deemed to be patentable as being based thereon.

In citing the references under Sec. 103(a), the question is raised whether the references would suggest

the invention, as stated in the decision of In Re Lintner (172 USPQ 560, 562, CCPA 1972);

> "In determining the propriety of the Patent Office case for obviousness in the first instance, it is necessary to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the references before him to make the proposed substitution, combination or other modification."

Similarly, In Re Regel (188 USPQ 136, CCPA 1975) decided that the question raised under Sec. 103 is whether the prior art taken as a whole would suggest the claimed invention to one of ordinary skill in the art. Accordingly, even if all the elements of a claim are disclosed in various prior art references, the claimed invention taken as a whole cannot be said to be obvious without some reason given in the prior art why one of ordinary skill would have been prompted to combine the teachings of the references to arrive at the claimed invention.

Simply put, and as stated in In Re Clinton (188 USPQ 365 CCPA 1976), "do the references themselves... suggest doing what appellants have done", such that there is a requirement that the prior art must have made any proposed modification or changes in the prior art obvious to do, rather than obvious to try.

It is respectfully put forward by the Applicant that there is no reason to consider the prior art references, Lauterbach, Hennessy and Culler, either individually or in combination, as rendering the invention obvious, since none of them discloses a four-step conversion process in which a first step comprises dividing each pipeline phase into a plurality n of sub-phases, a second step of creating n virtual pipelines comprising n*k sub-phases within existing pipeline, a third step of reproducing a register set, followed by a fourth step of adapting the

register set to enable simultaneous storing of the thread's machine states. The activities mentioned herein are performed on a computer processor configuration having a k-phased pipeline, thereby enabling conversion into a virtual processor having a register set and at least two threads.

In view of the foregoing remarks, all of the claims in the application are deemed to be allowable. Further reconsideration and allowance of the application is respectfully requested at an early date.

Respectfully submitted,

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